(Translation)

Mailed: February 24, 2004

NOTIFICATION OF REASONS FOR REJECTION

Patent Application No. : 2000-233129

Examiner's Notice Date : February 18, 2004

Examiner : SAKAMOTO Kunsyo

Attorney for Applicant: Mr. Takehiko Suzuye et al.

This application is rejected on the grounds stated below. Any opinion regarding this reason must be filed within SIXTY DAYS of the mailing date thereof.

REASONS

1. The inventions described in the following claims of the present application are unpatentable under Section 29(2) of the Patent Law, as being such that they could easily have been made by a person with ordinary skill in the art to which they pertain, on the basis of the invention described in the following distributed publication or made available to the public in Japan or elsewhere prior to this application.

REMARKS

Claims 1 to 5: see Reference 1.

Reference 1 discloses a probing method of a semiconductor integrated circuit wherein a test signal and a power supply signal are formed by a plurality of wiring traces.

The "step of supplying a test signal and a power supply signal quite independently of each other", the "step of supplying independently and concurrently", and the "step of measuring electric characteristics of a semiconductor integrated circuit chip quite independently and concurrently" as described in the specification of the divisional application are not in the coverage of the matters described in the specification or drawings originally attached to the present application, and do not